Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claims 1-60 (Canceled)

61. (Previously Presented) A refresh transition system for a dynamic random access memory ("DRAM") device having a plurality of rows of memory cells, the refresh transition system comprising:

a transitional refresh controller receptive of a refresh signal and an exit refresh signal, the transitional refresh controller being operable to ensure a refresh of at least one of the rows of memory cells responsive to receipt of the refresh signal, the transitional refresh controller ensuring refresh of the at least one of the rows of memory cells regardless of whether or not the transitional refresh controller receives the exit refresh signal before the refresh of the at least one of the rows of memory cells has occurred when the exit refresh signal is received.

62. (Previously Presented) The refresh transition system of claim 61 wherein the refresh signal comprises a self-refresh signal, and wherein the exit refresh signal comprises an exit self-refresh signal.

63. (Previously Presented) The refresh transition system of claim 61 wherein the transitional refresh controller initiates a refresh of the at least one of the rows of memory cells responsive to receiving the refresh signal and responsive to receiving the exit refresh signal.

64. (Previously Presented) The refresh transition system of claim 61 wherein the transitional refresh controller initiates a refresh of only one of the rows of memory cells responsive receiving the refresh signal.

65. (Previously Presented) The refresh transition system of claim 61 wherein the transitional refresh controller initiates a refresh of a plurality of the rows of memory cells responsive to receiving the refresh signal.

66. (Previously Presented) The refresh transition system of claim 61 wherein the transitional refresh controller initiates a refresh of all of the rows of memory cells in the DRAM device responsive to receiving the refresh signal.

67. (Previously Presented) The refresh transition system of claim 61 wherein the transitional refresh controller causes the DRAM device to switch to an operational mode responsive to receiving the exit refresh signal upon completion of a refresh of one of the rows of memory cells.

68. (Previously Presented) A refresh transition system for a dynamic random access memory ("DRAM") device having a plurality of rows of memory cells, the refresh transition system comprising:

a control circuit switching between a refresh mode and an operation mode, the control circuit being operable to ensure a refresh of at least one of the rows of memory cells each time the control circuit switches to the refresh mode regardless of whether or not at least one of the rows of memory cells has been refreshed when the control circuit switches to the operation mode.

69. (Previously Presented) The refresh transition system of claim 68 wherein the control circuit initiates a refresh of the at least one of the rows of memory cells responsive to both the control circuit switching to the refresh mode and the control circuit switching to the operation mode.

70. (Previously Presented) The refresh transition system of claim 68 wherein the control circuit initiates a refresh of only one of the rows of memory cells responsive to the control circuit switching to the refresh mode.

71. (Previously Presented) The refresh transition system of claim 68 wherein the control circuit controller initiates a refresh of a plurality of the rows of memory cells responsive to the control circuit switching to the refresh mode.

72. (Previously Presented) The refresh transition system of claim 68 wherein the control circuit initiates a refresh of all of the rows of memory cells in the DRAM device responsive to the control circuit switching to the refresh mode.

73. (Previously Presented) The refresh transition system of claim 68 wherein the control circuit causes the DRAM device to switch to the operation mode upon completion of a refresh of one of the rows of memory cells.

74. (Previously Presented) A refresh transition system for a dynamic random access memory ("DRAM") device having a plurality of rows of memory cells, the refresh transition system comprising:

a transitional refresh controller receptive of a refresh signal and an exit refresh signal, the transitional refresh controller being operable to refresh at least one of the rows of memory cells responsive to receipt of the refresh signal, the transitional refresh controller further being operable to transition the DRAM device to an operating mode responsive to receipt of the exit refresh signal as soon as one of the rows of memory cells is not being refreshed.

75. (Previously Presented) The refresh transition system of claim 74 wherein the refresh signal comprises a self-refresh signal, and wherein the exit refresh signal comprises an exit self-refresh signal.

76. (Previously Presented) The refresh transition system of claim 74 wherein the transitional refresh controller initiates a refresh of the at least one of the rows of memory cells responsive to receiving the refresh signal and responsive to receiving the exit refresh signal.

77. (Previously Presented) The refresh transition system of claim 74 wherein the transitional refresh controller initiates a refresh of only one of the rows of memory cells responsive receiving the refresh signal.

78. (Previously Presented) The refresh transition system of claim 74 wherein the transitional refresh controller initiates a refresh of a plurality of the rows of memory cells responsive to receiving the refresh signal.

79. (Previously Presented) The refresh transition system of claim 74 wherein the transitional refresh controller initiates a refresh of all of the rows of memory cells in the DRAM device responsive to receiving the refresh signal.

80. (Previously Presented) A dynamic random access memory ("DRAM") device comprising:

a plurality of rows of DRAM memory cells;

a row addressing system operably connected to the DRAM array, the row addressing system responsive to a row address signal by accessing a row in the DRAM array corresponding to the row address signal;

a column addressing system operably connected to the DRAM array, the column addressing system responsive to a column address signal by accessing a DRAM memory cell in a column of the DRAM array corresponding to the column address signal;

a row refreshing circuit operably connected with the row addressing system, the row refreshing circuit directing a refresh of at least one of the rows of DRAM memory cells in response to a refresh initiation signal;

a transitional refresh controller receptive of a refresh signal and an exit refresh signal, the transitional refresh controller being operable to generate the refresh initiation signal responsive to receipt of the refresh signal regardless of whether or not the transitional refresh controller has generated the refresh initiation signal when the transitional refresh controller receives the exit refresh signal; and

a data path operably coupling the DRAM array to an external data terminal of the DRAM device.

81. (Previously Presented) The DRAM device of claim 80 wherein the refresh signal comprises a self-refresh signal, and wherein the exit refresh signal comprises an exit self-refresh signal.

82. (Previously Presented) The DRAM device of claim 80 wherein the transitional refresh controller initiates a refresh of the at least one of the rows of DRAM memory cells responsive to receiving the refresh signal and responsive to receiving the exit refresh signal.

83. (Previously Presented) The DRAM device of claim 80 wherein the transitional refresh controller initiates a refresh of only one of the rows of DRAM memory cells responsive receiving the refresh signal.

84. (Previously Presented) The DRAM device of claim 80 wherein the transitional refresh controller initiates a refresh of a plurality of the rows of DRAM memory cells responsive to receiving the refresh signal.

85. (Previously Presented) The DRAM device of claim 80 wherein the transitional refresh controller initiates a refresh of all of the rows of DRAM memory cells in the DRAM device responsive to receiving the refresh signal.

86. (Previously Presented) The DRAM device of claim 80 wherein the transitional refresh controller causes the DRAM device to switch to an operational mode

responsive to receiving the exit refresh signal upon completion of a refresh of one of the rows of DRAM memory cells.

87. (Previously Presented) A dynamic random access memory ("DRAM") device comprising:

a plurality of rows of DRAM memory cells;

a row addressing system operably connected to the DRAM array, the row addressing system responsive to a row address signal by accessing a row in the DRAM array corresponding to the row address signal;

a column addressing system operably connected to the DRAM array, the column addressing system responsive to a column address signal by accessing a DRAM memory cell in a column of the DRAM array corresponding to the column address signal;

a row refreshing circuit operably connected with the row addressing system, the row refreshing circuit directing a refresh of at least one of the rows of DRAM memory cells in response to a refresh initiation signal;

a control circuit switching between a refresh mode and an operation mode, the control circuit being operable to ensure a refresh of at least one of the rows of DRAM memory cells each time the control circuit switches to the refresh mode regardless of whether or not at least one of the rows of DRAM memory cells has been refreshed when the control circuit switches to the operation mode; and

a data path operably coupling the DRAM array to an external data terminal of the DRAM device.

88. (Previously Presented) The DRAM device of claim 87 wherein the control circuit initiates a refresh of the at least one of the rows of DRAM memory cells responsive to both the control circuit switching to the refresh mode and the control circuit switching to the operation mode.

89. (Previously Presented) The DRAM device of claim 87 wherein the control circuit initiates a refresh of only one of the rows of DRAM memory cells responsive to the control circuit switching to the refresh mode.

90. (Previously Presented) The DRAM device of claim 87 wherein the control circuit controller initiates a refresh of a plurality of the rows of DRAM memory cells responsive to the control circuit switching to the refresh mode.

91. (Previously Presented) The DRAM device of claim 87 wherein the control circuit initiates a refresh of all of the rows of DRAM memory cells in the DRAM device responsive to the control circuit switching to the refresh mode.

92. (Previously Presented) The DRAM device of claim 87 wherein the control circuit causes the DRAM device to switch to the operation mode upon completion of a refresh of one of the rows of memory cells.

93. (Previously Presented) A dynamic random access memory ("DRAM") device comprising:

a plurality of rows of DRAM memory cells;

a row addressing system operably connected to the DRAM array, the row addressing system responsive to a row address signal by accessing a row in the DRAM array corresponding to the row address signal;

a column addressing system operably connected to the DRAM array, the column addressing system responsive to a column address signal by accessing a DRAM memory cell in a column of the DRAM array corresponding to the column address signal;

a row refreshing circuit operably connected with the row addressing system, the row refreshing circuit directing a refresh of at least one of the rows of DRAM memory cells in response to a refresh initiation signal;

a transitional refresh controller receptive of a refresh signal and an exit refresh signal, the transitional refresh controller being operable to refresh at least one of the rows of

DRAM memory cells responsive to receipt of the refresh signal, the transitional refresh controller further being operable to transition the DRAM device to an operating mode responsive to receipt of the exit refresh signal as soon as one of the rows of DRAM memory cells is not being refreshed; and

a data path operably coupling the DRAM array to an external data terminal of the DRAM device.

94. (Previously Presented) The DRAM device of claim 93 wherein the refresh signal comprises a self-refresh signal, and wherein the exit refresh signal comprises an exit self-refresh signal.

95. (Previously Presented) The DRAM device of claim 93 wherein the transitional refresh controller initiates a refresh of the at least one of the rows of memory cells responsive to receiving the refresh signal and responsive to receiving the exit refresh signal.

96. (Previously Presented) The DRAM device of claim 93 wherein the transitional refresh controller initiates a refresh of only one of the rows of memory cells responsive receiving the refresh signal.

97. (Previously Presented) The DRAM device of claim 93 wherein the transitional refresh controller initiates a refresh of a plurality of the rows of memory cells responsive to receiving the refresh signal.

98. (Previously Presented) The DRAM device of claim 93 wherein the transitional refresh controller initiates a refresh of all of the rows of memory cells in the DRAM device responsive to receiving the refresh signal.

99. (Previously Presented) A computer system, comprising:

a processor;

an input device operably connected to the processor allowing data to be entered into the computer system;

an output device operably connected to the processor allowing data to be output from the computer system; and

a system memory operably connected to the processor, the system memory comprising a plurality of dynamic random access memory ("DRAM") devices, each of the DRAM devices comprising:

a plurality of rows of DRAM memory cells;

a row addressing system operably connected to the DRAM array, the row addressing system responsive to a row address signal by accessing a row in the DRAM array corresponding to the row address signal;

a column addressing system operably connected to the DRAM array, the column addressing system responsive to a column address signal by accessing a DRAM memory cell in a column of the DRAM array corresponding to the column address signal;

a row refreshing circuit operably connected with the row addressing system, the row refreshing circuit directing a refresh of at least one of the rows of DRAM memory cells in response to a refresh initiation signal;

a control circuit switching between a refresh mode and an operation mode, the control circuit being operable to ensure a refresh of at least one of the rows of DRAM memory cells each time the control circuit switches to the refresh mode regardless of whether or not at least one of the rows of DRAM memory cells has been refreshed when the control circuit switches to the operation mode; and

a data path operably coupling the DRAM array to an external data terminal of the DRAM device.

100. (Previously Presented) The computer system of claim 99 wherein the refresh signal comprises a self-refresh signal, and wherein the exit refresh signal comprises an exit self-refresh signal.

101. (Previously Presented) The computer system of claim 99 wherein the transitional refresh controller initiates a refresh of the at least one of the rows of DRAM memory cells responsive to receiving the refresh signal and responsive to receiving the exit refresh signal.

102. (Previously Presented) The computer system of claim 99 wherein the transitional refresh controller initiates a refresh of only one of the rows of DRAM memory cells responsive receiving the refresh signal.

103. (Previously Presented) The computer system of claim 99 wherein the transitional refresh controller initiates a refresh of a plurality of the rows of DRAM memory cells responsive to receiving the refresh signal.

104. (Previously Presented) The computer system of claim 99 wherein the transitional refresh controller initiates a refresh of all of the rows of DRAM memory cells in the DRAM device responsive to receiving the refresh signal.

105. (Previously Presented) The computer system of claim 99 wherein the transitional refresh controller causes the DRAM device to switch to an operational mode responsive to receiving the exit refresh signal upon completion of a refresh of one of the rows of DRAM memory cells.

106. (Previously Presented) A computer system, comprising:

a processor;

an input device operably connected to the processor allowing data to be entered into the computer system;

an output device operably connected to the processor allowing data to be output from the computer system; and

a system memory operably connected to the processor, the system memory comprising a plurality of dynamic random access memory ("DRAM") devices, each of the DRAM devices comprising:

a plurality of rows of DRAM memory cells;

a row addressing system operably connected to the DRAM array, the row addressing system responsive to a row address signal by accessing a row in the DRAM array corresponding to the row address signal;

a column addressing system operably connected to the DRAM array, the column addressing system responsive to a column address signal by accessing a DRAM memory cell in a column of the DRAM array corresponding to the column address signal;

a row refreshing circuit operably connected with the row addressing system, the row refreshing circuit directing a refresh of at least one of the rows of DRAM memory cells in response to a refresh initiation signal;

a control circuit switching between a refresh mode and an operation mode, the control circuit being operable to ensure a refresh of at least one of the rows of DRAM memory cells each time the control circuit switches to the refresh mode regardless of whether or not at least one of the rows of DRAM memory cells has been refreshed when the control circuit switches to the operation mode; and

a data path operably coupling the DRAM array to an external data terminal of the DRAM device.

107. (Previously Presented) The computer system of claim 106 wherein the control circuit initiates a refresh of the at least one of the rows of DRAM memory cells responsive to both the control circuit switching to the refresh mode and the control circuit switching to the operation mode.

108. (Previously Presented) The computer system of claim 106 wherein the control circuit initiates a refresh of only one of the rows of DRAM memory cells responsive to the control circuit switching to the refresh mode.

109. (Previously Presented) The computer system of claim 106 wherein the control circuit controller initiates a refresh of a plurality of the rows of DRAM memory cells responsive to the control circuit switching to the refresh mode.

110. (Previously Presented) The computer system of claim 106 wherein the control circuit initiates a refresh of all of the rows of DRAM memory cells in the DRAM device responsive to the control circuit switching to the refresh mode.

111. (Previously Presented) The computer system of claim 106 wherein the control circuit causes the DRAM device to switch to the operation mode upon completion of a refresh of one of the rows of memory cells.

112. (Previously Presented) A computer system, comprising:

a processor;

an input device operably connected to the processor allowing data to be entered into the computer system;

an output device operably connected to the processor allowing data to be output from the computer system; and

a system memory operably connected to the processor, the system memory comprising a plurality of dynamic random access memory ("DRAM") devices, each of the DRAM devices comprising:

a plurality of rows of DRAM memory cells;

a row addressing system operably connected to the DRAM array, the row addressing system responsive to a row address signal by accessing a row in the DRAM array corresponding to the row address signal;

a column addressing system operably connected to the DRAM array, the column addressing system responsive to a column address signal by accessing a DRAM memory cell in a column of the DRAM array corresponding to the column address signal;

a row refreshing circuit operably connected with the row addressing system, the row refreshing circuit directing a refresh of at least one of the rows of DRAM memory cells in response to a refresh initiation signal;

a transitional refresh controller receptive of a refresh signal and an exit refresh signal, the transitional refresh controller being operable to refresh at least one of the rows of DRAM memory cells responsive to receipt of the refresh signal, the transitional refresh controller further being operable to transition the DRAM device to an operating mode responsive to receipt of the exit refresh signal as soon as one of the rows of DRAM memory cells is not being refreshed; and

a data path operably coupling the DRAM array to an external data terminal of the DRAM device.

113. (Previously Presented) The computer system of claim 112 wherein the refresh signal comprises a self-refresh signal, and wherein the exit refresh signal comprises an exit self-refresh signal.

114. (Previously Presented) The computer system of claim 112 wherein the transitional refresh controller initiates a refresh of the at least one of the rows of memory cells responsive to receiving the refresh signal and responsive to receiving the exit refresh signal.

115. (Previously Presented) The computer system of claim 112 wherein the transitional refresh controller initiates a refresh of only one of the rows of memory cells responsive receiving the refresh signal.

116. (Previously Presented) The computer system of claim 112 wherein the transitional refresh controller initiates a refresh of a plurality of the rows of memory cells responsive to receiving the refresh signal.

117. (Previously Presented) The computer system of claim 112 wherein the transitional refresh controller initiates a refresh of all of the rows of memory cells in the DRAM device responsive to receiving the refresh signal.

118. (Previously Presented) A method for transitioning a dynamic random access memory ("DRAM") device having a plurality of rows of memory cells between a refresh mode and an operating mode, comprising:

detecting when a processor-based system directs the DRAM device to transition to the refresh mode;

detecting when the processor-based system directs the DRAM device to transition to the operating mode; and

initiating a refresh of at least one of the rows of memory cells responsive to detecting that the computing system is directing the DRAM device to transition to the refresh mode regardless of whether or not at least one of the rows of memory cells has been refreshed when the processor-based system is directing the DRAM device to transition to the operating mode.

119. (Previously Presented) The method of claim 118 wherein the act of initiating a refresh of at least one of the rows of memory cells comprises initiating a refresh of at least one of the rows of memory cells responsive to both detecting that the processor-based system is directing the DRAM device to transition to the refresh mode and detecting that the processor-based system is directing the DRAM device to transition to the operating mode.

120. (Previously Presented) The method of claim 118 wherein the act of initiating a refresh of at least one of the rows of memory cells comprises initiating a refresh of only one of the rows of memory cells.

121. (Previously Presented) The method of claim 118 wherein the act of initiating a refresh of at least one of the rows of memory cells comprises initiating a refresh of a plurality of the rows of memory cells.

122. (Previously Presented) The method of claim 118 wherein the act of initiating a refresh of at least one of the rows of memory cells comprises initiating a refresh of all of the rows of memory cells in the DRAM device.

123. (Previously Presented) A method for transitioning a dynamic random access memory ("DRAM") device having a plurality of rows of memory cells between a refresh mode and an operating mode, comprising:

detecting when a processor-based system couples a refresh signal to the DRAM device;

detecting when the processor-based system couples an exit refresh signal to the DRAM device; and

ensuring a refresh of at least one of the rows of memory cells responsive to detecting the refresh signal regardless of whether or not the exit refresh signal is detected before the refresh of the at least one of the rows of memory cells has occurred when the exit refresh signal is detected.

124. (Previously Presented) The method of claim 123 wherein the refresh signal comprises a self-refresh signal, and wherein the exit refresh signal comprises an exit self-refresh signal.

125. (Previously Presented) The method of claim 123 wherein the act of ensuring a refresh of at least one of the rows of memory cells comprises ensuring a refresh of only one of the rows of memory cells.

126. (Previously Presented) The method of claim 123 wherein the act of ensuring a refresh of at least one of the rows of memory cells comprises ensuring a refresh of a plurality of the rows of memory cells.

127. (Previously Presented) The method of claim 123 wherein the act of ensuring a refresh of at least one of the rows of memory cells comprises ensuring a refresh of all of the rows of memory cells in the DRAM device.

128. (Previously Presented) The method of claim 123, further comprising transitioning the DRAM device to an operational mode responsive to detecting that the processor-based system has coupled the exit refresh signal to the DRAM device.

129. (Previously Presented) A method for transitioning a dynamic random access memory ("DRAM") device having a plurality of rows of memory cells between a refresh mode and an operating mode, comprising:

detecting when a processor-based system couples a refresh signal to the DRAM device;

detecting when the processor-based system couples an exit refresh signal to the DRAM device;

detecting when none of the rows of memory cells in the DRAM device is being refreshed;

refreshing at least one of the rows of memory cells responsive to detecting the refresh signal; and

transitioning the DRAM device to an operating mode responsive to detecting the exit refresh signal and detecting that none of the rows of memory cells is being refreshed.

130. (Previously Presented) The method of claim 129 wherein the refresh signal comprises a self-refresh signal, and wherein the exit refresh signal comprises an exit self-refresh signal.

131. (Previously Presented) The method of claim 129 wherein the act of refreshing at least one of the rows of memory cells responsive to detecting the refresh signal comprises refreshing only one of the rows of memory cells responsive to detecting the refresh signal.

132. (Previously Presented) The method of claim 129 wherein the act of refreshing at least one of the rows of memory cells responsive to detecting the refresh signal comprises refreshing a plurality of the rows of memory cells responsive to detecting the refresh signal.

133. (Previously Presented) The method of claim 129 wherein the act of refreshing at least one of the rows of memory cells responsive to detecting the refresh signal comprises refreshing all of the rows of memory cells in the DRAM device responsive to detecting the refresh signal.